PC FUNCTION GNERATOR K8016

Description of operation

The shift registers IC2, IC3, IC19 and IC21 store the setup data controlling the operations of the generator. The 32-bit data word to these registers is fed in serial mode via optocoupler IC37 from the printer port connector J7. The clock to the shift registers is fed via optocoupler IC20 and the PAL circuit IC22.

Before transferring the data the optocoupler input supply voltage must be turned on by pulling pin 17 of connector J7 down. The supply voltage to the optocouplers is fed from the printer port data lines via 8 diodes and transistor T8.

Signals C0 and C1 connected from optocouplers IC35 and IC36 to IC22 are used to control the function of the outputs of IC22. The status of this pins is valid (and shifted to the output pins 14 and 15 of IC22) after the CLK rising edge to pin 1 of IC22.

C0	**C1**	**Operation mode**
0	0	Run mode
1	0	RCK2 goes high at the rising edge of the CLK to pin 1 of IC22. Data will be latched to the shift register IC5.
0	1	RCK1 goes high at the rising edge of the CLK to pin 1 of IC22. Data will be latched to the shift registers IC2 ... IC21.
1	1	Data transfer mode

Loading the shift registers

Inputs			**Outputs**		**Data bit name**	**Note**
C0	C1	CLK	CLK1	RCK1		
1	1	0	0	0		
1	1	1	0	0	ENABLE1	
1	1	0	1	0	ENABLE1	First data bit shifted to the shift register
1	1	1	0	0	S14	
1	1	0	1	0	S14	
1	1	1	0	0	...	Repeat the data send operation. Bit sent to the shift register at the falling edge of CLK
1	1	0	1	0	...	
1	1	1	0	0	DC0	
1	1	0	1	0	DC0	Last data bit shifted to the shift register
0	1	1	0	1		Data moved and latched to the outputs of the shift registers IC2 ... IC21

The waveform data is transferred in serial mode to the shift register IC5 and then moved to the SRAM IC10. The address counter is incremented before each data movement to IC10.

Loading the wave data to the SRAM

Inputs			Outputs					Data bit	Note
C0	C1	CLK	CLK1	RCK2	WE	OE1	COUNT		
1	1	0	0	0	1	0	0		.
1	1	1	0	0	1	0	0	DB7	ENABLE output of IC22 goes low.
1	1	0	1	0	1	0	0	DB7	First data bit shifted to the shift register IC5
1	1	1	0	0	1	0	0	DB6	
1	1	0	1	0	1	0	0	DB6	
1	1	1	0	0	1	0	0	...	Repeat the data send operation
1	1	0	1	0	1	0	0	...	
1	1	1	0	0	1	0	0	DB0	
1	1	0	1	0	1	0	0	DB0	Last data bit shifted to the shift register
1	0	1	0	1	1	0	1		Data moved and latched to the outputs of the shift register IC5. Address counter incremented
1	0	0	0	1	0	0	1		Data byte written to the RAM from IC5 output
The sequence above is repeated until all the data bytes are transferred to the RAM									
0	0	0	0	1	0	0	0		
0	0	1	0	0	1	1	0		RAM outputs are now enabled. ENABLE output of IC22 goes high. Selected clock rate is output from COUNT.

Shift register content

IC2: Offset voltage control register

Pin no.	Signal name	Description
15	DC0	Controls the offset voltage 00000000 = $00 = -5V 01111111 = $7F = 0V 11111111 = $FF = +5V
1	DC1	
2	DC2	
3	DC3	
4	DC4	
5	DC5	
6	DC6	
7	DC7	

IC3: Operation mode control register

Pin no.	Signal name	Description
15	RESET	LO = Resets the address counters IC48, IC49, IC50 and IC7
1	TR_SEL	LO = Triggering occurs at the start of the sequence HI = Trigger signal is square wave formed output signal
2	SEL_F0	Sample rate frequency selection and filter selection
3	SEL_F1	
4	SEL_F2	
5	AMPL0	Output attenuator selection
6	AMPL1	
7	AMPL2	

Sampling frequency selection

SEL_F0	SEL_F1	SEL_F2	Sample rate	Output filter
0	0	0	32 MHz	OFF
1	0	0	3.2 MHz	ON
0	1	0	320 kHz	ON
1	1	0	32 kHz	ON
0	0	1	3.2 kHz	ON
1	0	1	320 Hz	ON
0	1	1	32 MHz	ON
1	1	1	32 MHz	ON

Output voltage range selection

AMPL0	AMPL1	AMPL2	Peak output voltage
0	0	0	0.078125 Vpp (not used)
1	0	0	0.15625 Vpp
0	1	0	0.3125 Vpp
1	1	0	0.625 Vpp
0	0	1	1.25 Vpp
1	0	1	2.5 Vpp
0	1	1	5 Vpp
1	1	1	10 Vpp

IC19: Address counter start address in run mode.

Pin no.	Signal name	Description
15	S00	Low byte of the address counter start address.
1	S01	
2	S02	
3	S03	
4	S04	
5	S05	
6	S06	
7	S07	

IC21: Address counter start address in run mode and filter on/off control.

Pin no.	Signal name	Description
15	S08	High byte of the address counter start address.
1	S09	
2	S10	
3	S11	
4	S12	
5	S13	
6	S14	
7	ENABLE	LO = Output filter off, HI = Output filter on

Wave data calculation

The wave data is stored to the SRAM IC10. In run mode the data is output from the RAM at the clock sample rate. The data is fed to the D/A converter IC6.

There are 6 different sample rates available (320 Hz to 32 MHz). The output frequency depends the number of wave cycles stored to the RAM and the start count of the address counters.

Some examples:

1. We want to generate 1.0 kHz frequency using 32 MHz sample rate.
Dividing the sampling frequency by the wanted output frequency we get the number of samples needed to output one cycle of 1.0 kHz.

N = 32000 kHz / 1 kHz
= 32000 samples / cycle

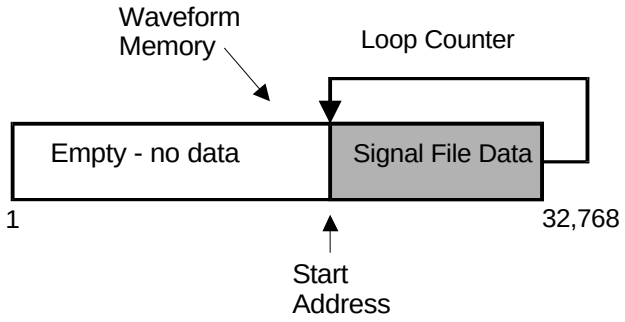
2. Now we like to generate 1.25 kHz frequency.

N = 32000 / 1.25
= 25600 samples / cycle

3. Now we like to generate 999 kHz frequency.

N = 32000 / 999
N = 32.032 samples / cycle

Only integer values are possible for the sample count.
In this case we have to put more than one cycle of the data to the memory. The samples per cycle value must be multiplied to get integer value.
In this case multiplying the samples per period number by 999 gives us an integer value of 32000.
In this case we fill the memory with 999 periods of the data. The data is put to the upper end of the memory. The start address of the address counter is set to a value that only the data upper 999 addresses are sent to the D/A converter.



Using the debug version of the function generator software you'll see how many periods of data is stored to the memory. In some cases the software has to average the number of samples to the nearest integer value. This causes a little error to the output frequency. The debug software displays also this error in %.
Anyhow the maximum frequency setting error is always less than 0.01%.

The following code fragment demonstrates the technique of generating the number of samples and number of periods to be put to the memory:

```
                    {f = frequency in kHz}
  j1:=1;
  min:=1;
  fk:=32000/f;          {fk = count of samples/cycle}

  {Next loop calculates the number of cycles for the best fit}

  for j:=1 to 1000 do     {j = number of cycles}
  begin
    s:=j*fk;              {s = total number of samples}
    if rr<=32766 then
    begin
      fout:=32000*j/round(s);    {fout = real output frequency}

      if fout>= f then d:=fout-f else d:=f-fout;
      if (d<min) then
      begin
        i1:=round(rr);    {i1 = count of samples}
        j1:=j;            {j1 = count of periods}
        min:=d;
      end;
    end;
  end;
```

Waveform generation

The address generator sequentially presents data values from each memory location to the digital-to-analog converter.
The waveform generator will output all the points in the waveform at the sample clock rate specified. The resulting frequency is equal to the sample clock rate divided by the number of data points in the waveform. If multiple cycles of the waveform are entered into the same waveform memory space, the output frequency will increase proportional to the number of cycles in memory.

Number of samples per cycle

The waveform you create in the Wave Editor or by other means is a series of data points.
All the data points make up one function generator output cycle. The function generator attempts to output all the points at the frequency you specify. At the higher frequencies the generator automatically samples the points so the full waveform is output. You'll see the sampled waveform in the output wave preview window.

Range / Hz	Output frequency	Number of samples per cycle
0.1	10mHz	32000
	100mHz	3200
1	0.1Hz	32000
	1Hz	3200
10	1Hz	32000
	10Hz	3200
100	10Hz	32000
	100Hz	3200
1k	100Hz	32000
	1000Hz	3200
10k	1000Hz	32000
	10000Hz	3200
100k	10kHz	3200
	100kHz	320
1M	100kHz	320
	1000kHz	32

Trigger pulse generation

The triggering output square pulse is achieved on every cycle for sine, square, triangle, sine(x)/x and library waveforms. A zero crossing detector (T9, T10) is used to form a square wave. This signal TR_1 is fed via the NAND gates IC15B and IC15C to the trigger output.

For sweep and noise the triggering pulse is generated at the beginning of each sequence. This pulse is generated by discharging the capacitor C5 via diode D14 when the address counter reaches it’s final count. The discharge pulse width is about 31 ns. This pulse is too short for triggering purposes. The pulse is width is extended by charging the capacitor C5 via a charge pump consisting of the diodes D15, D16 and capacitor C6. The charge time depends on the frequency range selected. The output pulse width is always about equal to the width of ten clock (COUNT) pulses.

Voltage of C5 and the trigger pulse when the sample rate is 320kHz.