PC-OSCILLOSCOPE PCS500

Analog and digital circuit sections

Description of the operation

Operation of the analog section

This description concerns only channel 1 (CH1) input stages. The operation of CH2 is similar.

The signal is applied to the input attenuator either via relay contact RY1 or via capacitor C4. The relay is used to select the type of input connection, AC or DC. If DC connection is selected the input signal is directly connected to the input attenuator. This position is probably the mainly used input connection type. Both DC and AC components of the signal can be measured and displayed on the screen. If AC coupling is selected the input signal passes through a 47 nF capacitor C4 to the input attenuator. The capacitor blocks DC component of the input signal to pass to the input circuit. Also AC signals at very low frequencies are blocked. The low frequency limit is about 5 Hz (at -3dB). The AC position is useful if low amplitude AC signals over a rather high DC voltage have to be measured. If, for example, an AC ripple voltage of a DC power supply must be measured.

Next to the input coupling selector there is a frequency-compensated voltage divider (R6, R12, R13). To adjust the frequency response of the attenuator there are two trimmer capacitors CV5 and CV6. A square wave obtained from the test connector J9 (at the rear of the scope) can be used to help the adjustment of the trimmers.

The attenuation ratios are 1:1, 1:10 and 1:100.

The attenuator output is selected by the relays RY2, RY3 and RY4. Relay RY5 is used to connect the input of the following amplifier to ground. When input selector position "GND" is selected all of the relays RY2, RY3 and RY4 are open and the input of the amplifier is grounded via RY5.

Overvoltage protection of the input amplifier is made with resistor R30 and the diodes D10 and D14. This circuit limits the maximum voltage at the gate of the FET T1A to the level of +/-5.5V.

Fet T1B provides a constant current source for T1A. Trimmer RV3 is used to adjust the constant current to the level that the voltage across R4 is exactly same as the gate-source voltage of T1A plus the offset voltage of amplifier IC2A. When this adjustment is correctly done then the gain change of the amplifier IC2A doesn't cause any jump to it's output voltage if zero voltage is connected to the input connector of the scope.

The gain of the amplifier IC2A is set by the relay RY6. The gains are x1 and x10.

The gain of the second amplifier stage IC2B is set by the relay RY7. The gains of this stage are x0.833 and x 2.5.

The Y-position of the trace is adjusted by feeding DC current from the collector of the transistor T8 to the inverting input of IC2B. The current is set by the output voltage OFFS_1 of the D/A converter IC26.

Finally the signal is fed to the A/D converter IC16 via the emitter follower T10 and R115. Transistor T3 provides a constant current source for T10.

The emitter follower transistor T10 has two functions. First, it shifts the output voltage of the amplifier IC2B about 0.6 V upwards, this is needed because the A/D-converter IC19 operates between 0V and +5V and the amplifier operates between -5V and +5V. Secondly, it prevents together with the diode D12 and resistor R48 the input voltage of the A/D-converter to go below 0V.

The final gain adjustment is done with the trimmer RV1.

The operation of the A/D-converter is controlled by the AD_CLK signal. The conversion occurs at the rising edge of the signal.

Operation of the digital section

The digital section consist of the following functional blocks:
1. Clock oscillator X1, pre-divider IC18 and programmable frequency divider IC8... IC11.
2. Shift registers as a storage of the 16 bit control word IC4...IC7
3. Clock signal distributor PLD circuit IC22 (includes also some other functions).
4. Address and pre trigger counters IC48...IC50
5. Post trigger counters IC12...IC14 (counts 3072 pulses after the occur of the triggering).
6. Data storage memory IC51 and IC52
7. Output multiplexer IC53 and IC54, transfer the digitized data to the PC via the printer port in groups of 4 bits
8. Output multiplexer selector IC21B

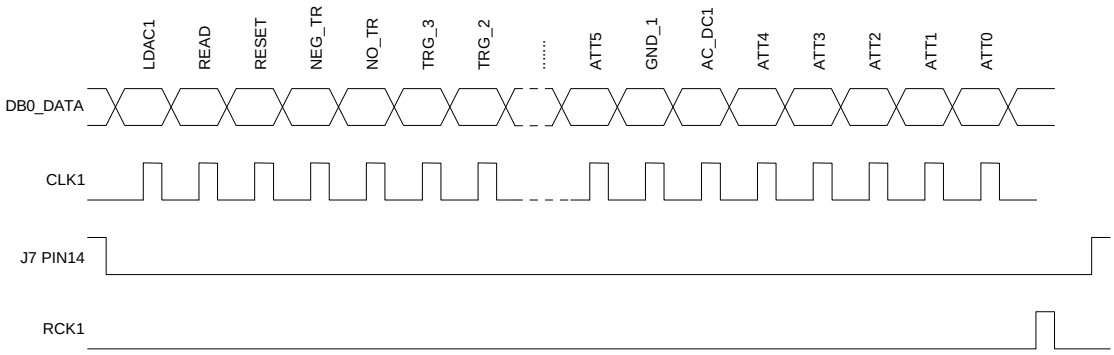
The 50 MHz clock signal is fed via a pre-divider flip-flops IC18A and IC18B (divide by 4) to the and programmable frequency divider IC8... IC11. This divider outputs the desired clock frequency. The output signal of the divider is fed via the PLD circuit IC22 as a sampling clock to the A/D-converters (signal AD_CLK), to memory address counters (COUNT_F), to the post trigger counters (COUNT) and to the memory as a write enable signal (WE).

The shift registers IC4...IC7 store the setup data controlling all the operations of the oscilloscope unit. The data and clock inputs to these registers are fed via the buffer circuit IC16B and the optocouplers from the parallel printer port connector J7.

Before transferring the data the buffer circuit IC16 must be enabled by pulling pin 14 of connector J7 down. The supply voltage to IC16 is fed via the printer port data lines. All the data lines that are not in use must be held high all the time.

The data to the shift registers is fed via pin 2 and the transfer clock via pin 3 of J7. A high-to-low transition to pin 3 causes the serial data to be shifted into the shift registers.

When all the 32 bits of the data are shifted to the registers it's time to latch the data to the outputs of the shift registers. This is done by pulling pin 5 of J7 down and back to high.



Loading the shift registers

Shift register content

IC4: Channel 1 input attenuator and amplifier gain is controlled by IC4

PIN NO.	SIGNAL NAME	DESCRIPTION
15	ATT0	Ch1 input attenuator setting
1	ATT1	Ch1 input attenuator setting
2	ATT2	Ch1 input attenuator setting
3	ATT3	Ch1 input amplifier gain setting
4	ATT4	Ch1 input amplifier gain setting
5	AC_DC1	Ch1 input AC/DC coupling : LO = DC coupling, HI = AC coupling
6	GND_1	Ch1 input GND coupling: LO = GND, HI = normal operation
7	(POWER_OFF)	Power supply control: LO = power on, HI = power off

IC5: Channel 2 input attenuator and amplifier gain is controlled by IC5

PIN NO.	SIGNAL NAME	DESCRIPTION
15	ATT5	Ch2 input attenuator setting
1	ATT6	Ch2 input attenuator setting
2	ATT7	Ch2 input attenuator setting
3	ATT8	Ch2 input amplifier gain setting
4	ATT9	Ch2 input amplifier gain setting
5	AC_DC2	Ch2 input AC/DC coupling : LO = DC coupling, HI = AC coupling
6	GND_2	Ch2 input GND coupling: LO = GND, HI = normal operation
7		

IC6: The data controlling the operation of the clock frequency divider is stored to the shift register IC6.

PIN NO.	SIGNAL NAME	DESCRIPTION
15	F0	IC8 divider control: LO = divide by 10, HI = divide by 5 (F1 = LO)
1	F1	IC8 divider control: HI = divide by 2 (F0 = LO)
2	F2	IC9 divider control: LO = divide by 10, HI = divide by 1
3	F3	IC10 divider control: LO = divide by 10, HI = divide by 1
4	F4	IC11 divider control: LO = divide by 10, HI = divide by 1
5	F5	IC22 output frequency control for COUNT, AD_CLK and WE
6	F6	IC22 output frequency control for COUNT, AD_CLK and WE
7		

IC7: Triggering and data reading from the scope is controlled by IC7

PIN NO.	SIGNAL NAME	DESCRIPTION
15	TRG_1	Trigger input selection: HI = CH1 (TRG_2 = LO, TRG_3 = LO)
1	TRG_2	Trigger input selection: HI = CH2 (TRG_1 = LO, TRG_3 = LO)
2	TRG_3	Trigger input selection: HI = EXT (TRG_1 = LO, TRG_2 = LO)
3	NO_TR	Trigger on/off selection: LO = on, HI = off
4	NEG_TR	Trigger edge selection for CH1 and CH2: LO = positive, HI = negative Trigger edge selection for Ext. Trig.: LO = negative, HI = positive
5	RESET	Reset all address counters: LO = reset, HI = run
6	READ	Enables data reading from the scope: LO = data read enabled, HI = acquire data
7	LDAC1	Controls the data update to the D/A converters: LO = D/A data updated

The states of the outputs of IC6 at different Time/div settings are following:

DSO Time/Div.	FFT Freq. Range	F6	F5	F4	F3	F2	F1	F0	Sampling frequency
20 ns		0	0	0	0	0	0	0	50 MHz
50 ns		0	0	0	0	0	0	0	50 MHz
100 ns		0	0	0	0	0	0	0	50 MHz
200 ns		0	0	0	0	0	0	0	50 MHz
0.1 us		0	0	0	0	0	0	0	50 MHz
0.2 us		0	0	0	0	0	0	0	50 MHz
0.5 us		0	0	0	0	0	0	0	50 MHz
1 us		0	0	0	0	0	0	0	50 MHz
2 us		0	0	0	0	0	0	0	50 MHz
5 us	25 MHz	0	0	0	0	0	0	0	50 MHz
10 us	12 MHz	0	1	0	0	0	0	0	25 MHz
	6 MHz	1	0	0	0	0	0	0	12.5 MHz
20 us	3 MHz	1	1	1	1	1	1	0	6.25 MHz
50 us	1.2 MHz	1	1	1	1	1	0	1	2.5 MHz
0.1 ms	0.6 MHz	1	1	1	1	1	0	0	1.25 MHz
0.2 ms	300 kHz	1	1	1	1	0	1	0	625 kHz
0.5 ms	120 kHz	1	1	1	1	0	0	1	250 kHz
1 ms	60 kHz	1	1	1	1	0	0	0	125 kHz
2 ms	30 kHz	1	1	1	0	0	1	0	62.5 kHz
5 ms	12 kHz	1	1	1	0	0	0	1	25 kHz
10 ms	6 kHz	1	1	1	0	0	0	0	12.5 kHz
20 ms	3 kHz	1	1	0	0	0	1	0	6.25 kHz
50 ms	1.2 kHz	1	1	0	0	0	0	1	2.5 kHz
100 ms		1	1	0	0	0	0	0	1.25 kHz

The states of the outputs of IC4 at different Volts/div settings are following:

Volts/Div. range	ATT4	ATT3	ATT2	ATT1	ATT0	Input attenuator	IC2A gain	IC2B gain	Total gain from input to IC19
15 V	1	1	0	1	1	100	1	0.833	0.00833
5 V	0	1	0	1	1	100	1	2.5	0.025
1.5 V	1	1	1	0	1	10	1	0.833	0.0833
0.5 V	0	1	1	0	1	10	1	2.5	0.25
0.15 V	1	1	1	1	0	1	1	0.833	0.833
50 mV	0	1	1	1	0	1	1	2.5	2.5
15 mV	1	0	1	1	0	1	10	0.833	8.33
5 mV	0	0	1	1	0	1	10	2.5	25

The full-scale input voltage range to the A/D converter is 1V.

The PC displays eight vertical divisions on the screen.
For example at 5 mV/div range the max peak-to-peak value displayed on the screen is 8 x 5 mV = 40 mV.
The needed gain is 1V / 40 mV = 25.

Reset

The data acquiring starts immediately after the reset. This is done by pulling pin 5 (RESET) of IC7 down and back up. This operation reset all the address counters, trigger flip-flop IC25 and the outputs of IC22.

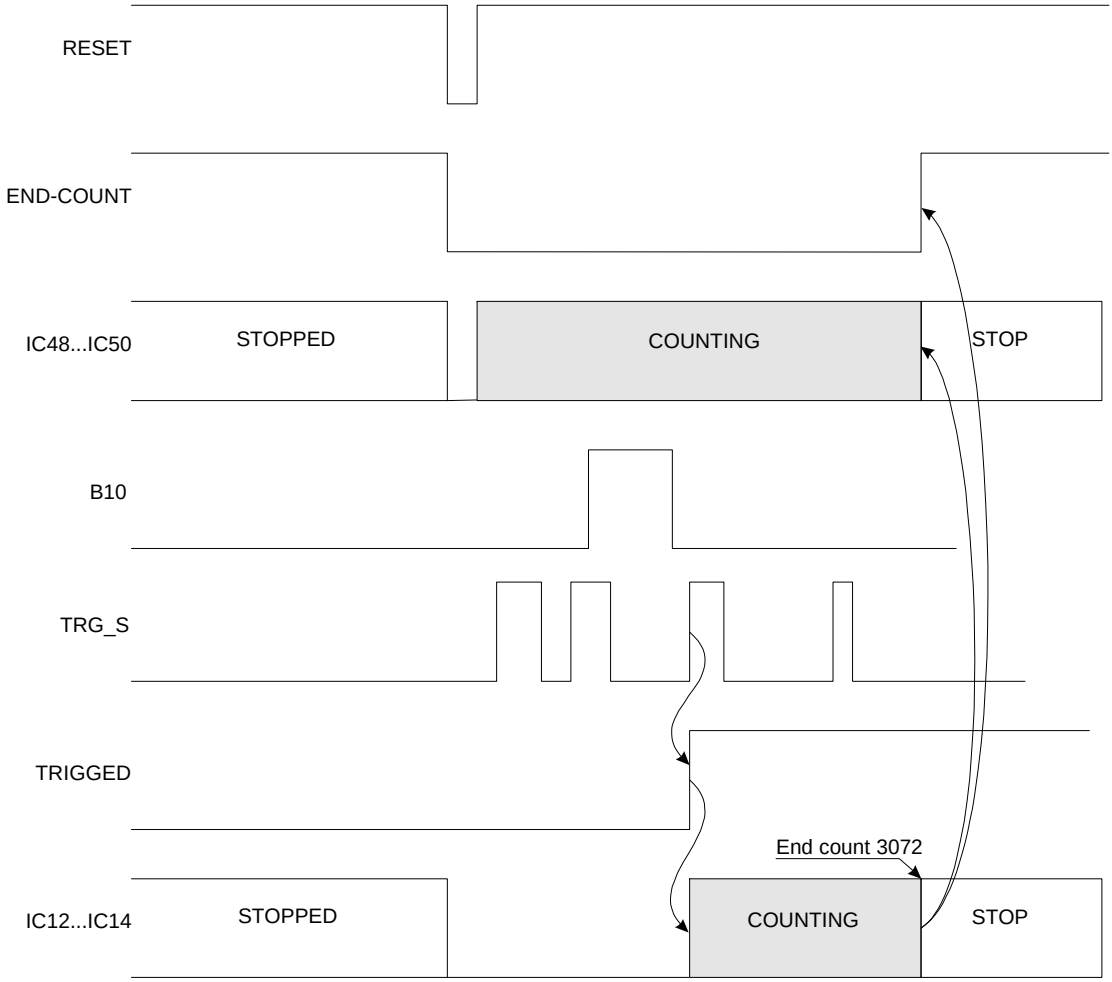
Acquire

The address counters IC48...IC50 begin to count and the A/D converters IC19 and IC27 start to convert the analog input signals to digital form. The data is stored to the consecutive addresses of the RAM circuits IC51 and IC52.

When address counter reaches the count 1024 goes the address line B10 high. This sets flip-flop IC25A and allows triggering to occur because enough data prior to the triggering point is now stored to the memory. If TRIG ON button is selected, the triggering occurs when the output pin 4 of the trigger comparator IC32 changes its state. (The signal of the selected trigger channel passes the triggering level.) Depending on the trigger slope selection, IC22 generates a positive going pulse to its output pin 18 (TRG_OUT). This set flip-flop IC25B. After this, at the next clock pulse the output 22 (TRIGGED) of IC22 will be set high.

Now the counters C12...IC14 are allowed begin to count. This state stays until the END_C1 signal from the pin 11 of IC15D goes low. This happens when the post trigger counters IC12...IC14 reach the count of 3072. This is the count of samples stored to the memory after the triggering point. Now total amount, 4096 samples are stored to the memory; 1024 before the triggering point and 3072 samples after the triggering point.

If TRIG-OFF button is selected, then IC22 gives continuous train of the clock pulses to the output TRG_OUT. In this case the triggering happens immediately after the first 1024 values from the A/D converters are stored to the memory.



Reset and data digitizing cycle

Data read

Now it is time to read the data from the RAMs IC51 and IC52 to the PC. First the READ signal at pin 6 of IC7 must be pulled down. This enables the RAM outputs and disconnects the A/D converters from the data bus by the analog switches IC28, IC33, IC34 and IC36. Trigger comparator is also disabled and the 2-to-4-line decoder IC21B is enabled.

The data reading from the RAM happens in groups of 4-bits. The data is transferred to the parallel printer port data input via the circuits IC53 and IC54. The 2-to-4-line decoder IC21B is used to select the output 4-bit group. After reading all four groups from the RAM the input 6 (DB2_LOAD) of PLD circuit IC22 should be taken high and back to low. This pulse is directly transferred to the output 14 of IC22 (COUNT_F) and forwarded to the address counter IC48...IC50 input. This happens only if the output 20 of IC22 (END_COUNT) is high. The pulse increments the address counters IC48...IC50 and next memory location can be read.

After all the data is read (2x4096 bytes) the program sends RESET to the address counters and the operation described above will be repeated.

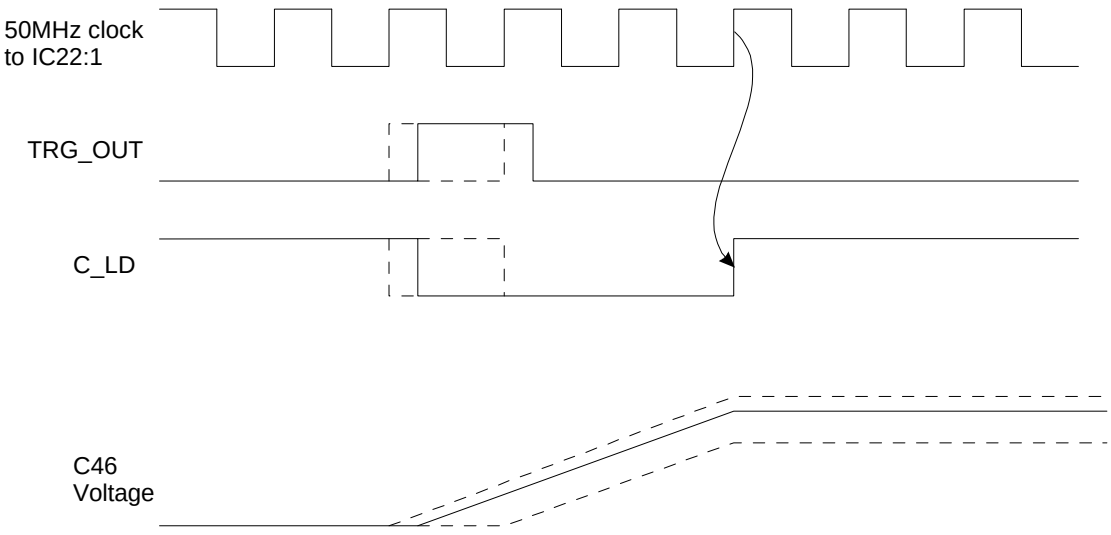
Random Repetitive Sampling mode

This mode can be used only for repetitive signals. When a trigger event occurs, the oscilloscope measures the time from the trigger event to the next sample. Knowing this time allows the oscilloscope software to assign the samples to the correct time relative to the trigger for that occurrence. On each occurrence of the signal, more points are acquired. After enough trigger events have occurred, the waveform is completely defined.

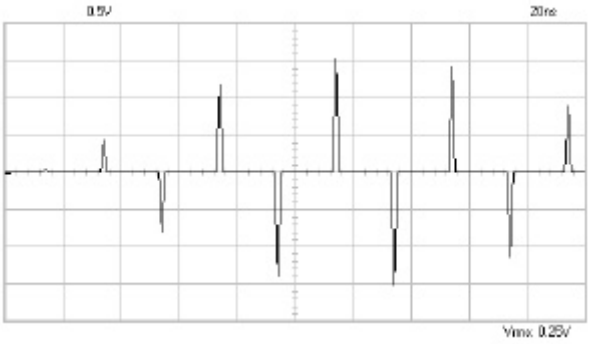
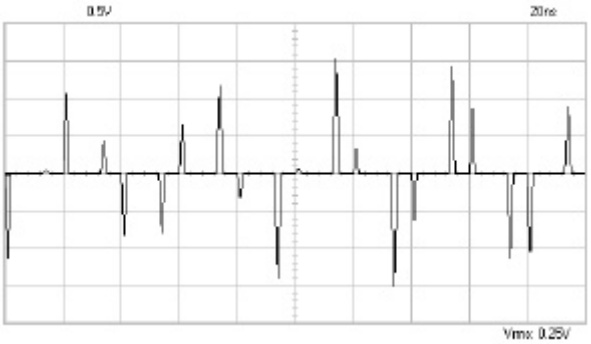
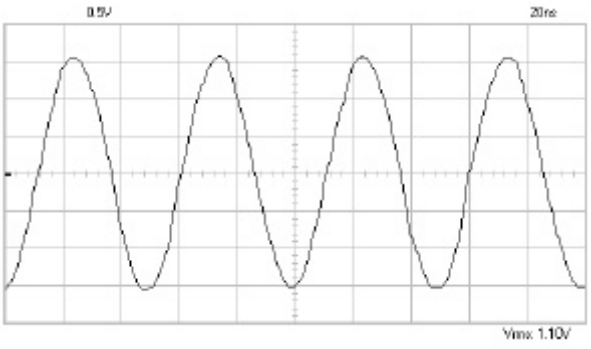
When triggering occurs the output pin 8 of IC25B goes low. This pulls the base of transistor T5 to zero. A constant current through T5 starts to charge C46. This continues until the second clock pulse after the triggering occurrence has arrived to the PAL circuit IC22. This resets IC25B by pulling its pin 13 (C_LOAD) down. Capacitor C46 keeps its charge until it is discharged via the analog switch IC35.

The voltage of C46 is read before it is discharged. This is done comparing its voltage value to the voltage generated by the D/A converter IC26. The voltage of C46 is magnified by 6 by IC24B and fed to the input of comparator IC32. The voltage generated by D/A converter IC26 to it's output pin 11 (C_VOLTS) is fed via buffer amplifier IC24A to comparator IC32. The output pin 9 (TIME_1) of comparator IC32 is connected via optocoupler IC43 and line driver IC16A to pin 12 of the LPT connector J7. If the voltage of PIN 12 of IC32 is higher than the voltage of pin 11 then the output 11 of IC32 and the state of LPT connector pin 12 is HIGH. By monitoring the state if this pin and adjusting the output voltage of IC26 the voltage of C46 can be determined.

The digitized samples are stored to the waveform display buffer memory locations based on the voltage of C46. This is done by comparing the voltage of C46 to the accumulated max and min voltages of C46 during the session. This voltage range is divided to 20 segments. This means that there are 20 different locations for the samples (oversample rate is 1GHz = 20 x 50MHz).



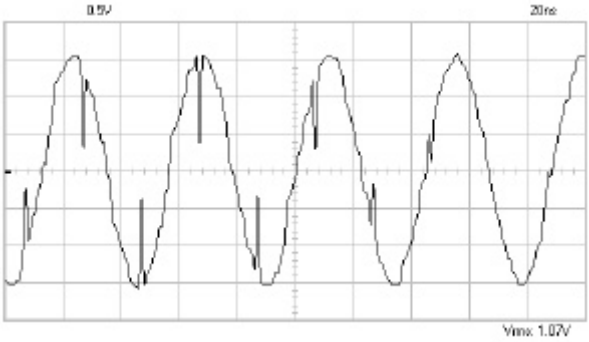
Charging the C46

The steps of the operation in Random Repetitive Sampling mode
• Data is stored to PCS500 hardware SRAM: • 1KB before the triggering • 3KB after the triggering
• The time (T) from the trigger event to the next sample is measured
• 200 Bytes of data is read from the PCS500 SRAM to PC's temporary memory buffer. • The data is distributed to the memory starting at the offset based on time (T). • The space between the samples is 20 address locations.

After next triggering the steps above are repeated and another group of 200 samples is placed to the temporary memory.

After enough trigger events have occurred, the waveform is completely defined.


There are two steps done before the data is moved from the temporary memory to the display buffer:

1. Averaging

Because the samples are gathered randomly it may sometimes take rather long time until all 20 positions of the waveform data are collected. In this case the waveform may look like this:

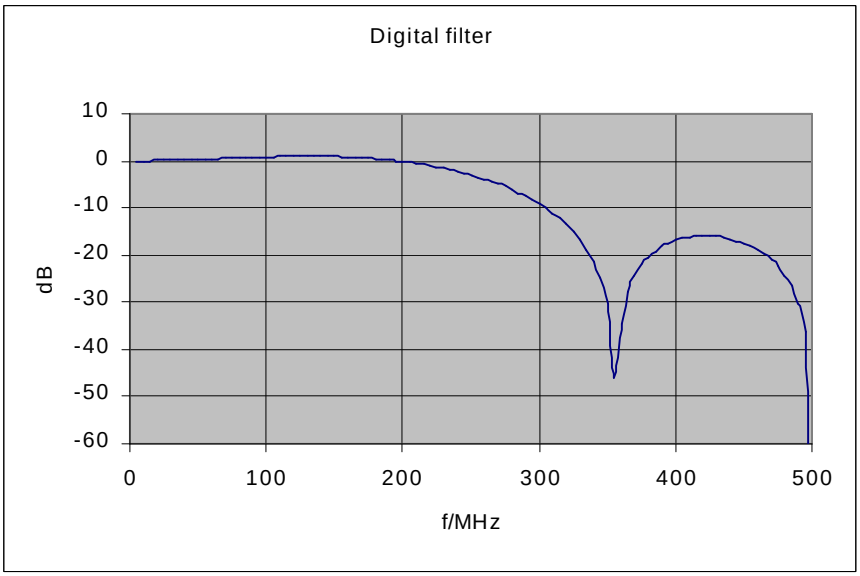


One sample is missing

To speed up the trace stabilization the missing samples are replaced with the samples created by calculating an average of the two adjacent samples.

2. Digital filtering

Finally the data is fed via a digital filter that removes the unwanted higher frequencies of the displayed waveform.

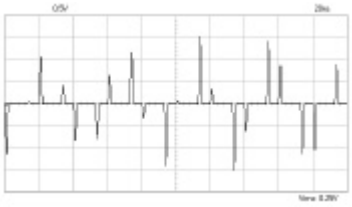
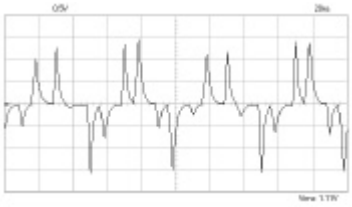
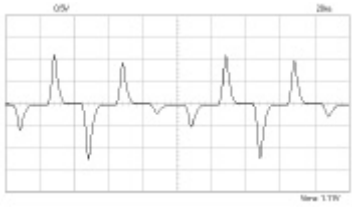
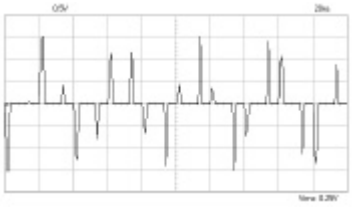
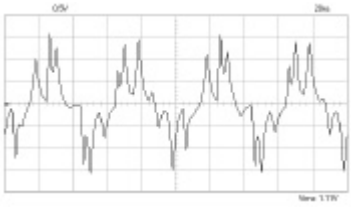
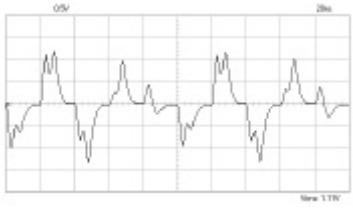
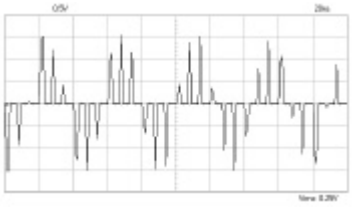
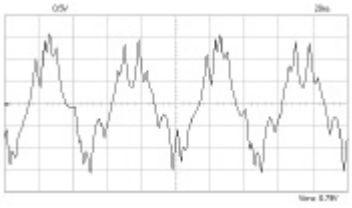
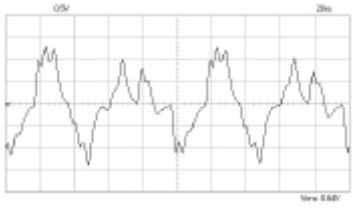
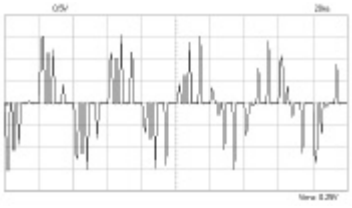
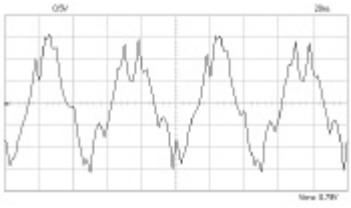
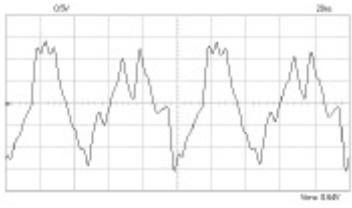
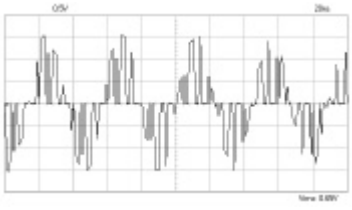
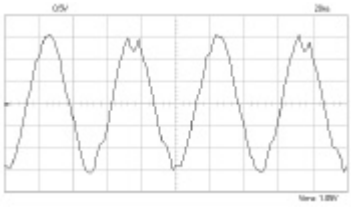
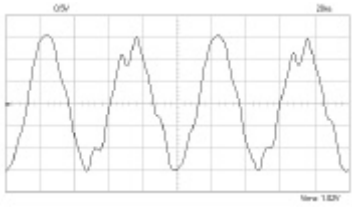


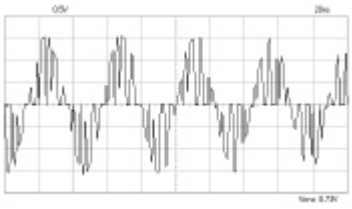
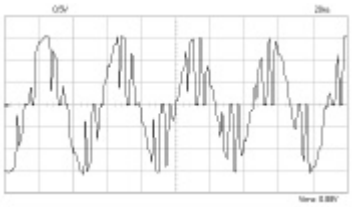
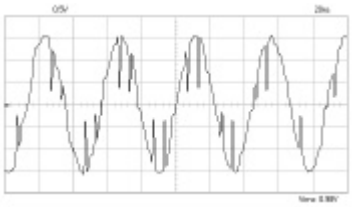
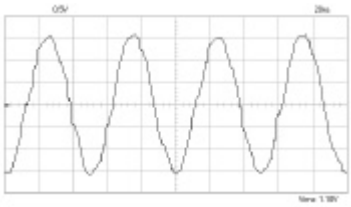
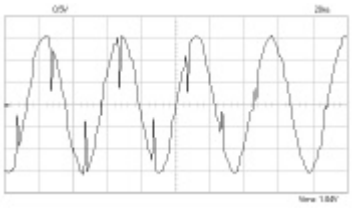
The frequency response of the digital filter

The advantage of these methods can be clearly seen in the images below.

The development of a waveform during random repetitive sampling

The same signal after 1 to 50 acquisitions without any improvements, with averaging and with averaging and filtering.

Raw data	Missing samples replaced with average of adjacent samples	Average + Digital filter
After 1 sample		
		
After 2 samples		
		
After 3 samples		
		
After 4 samples		
		
After 5 samples		
		
After 10 samples		
		

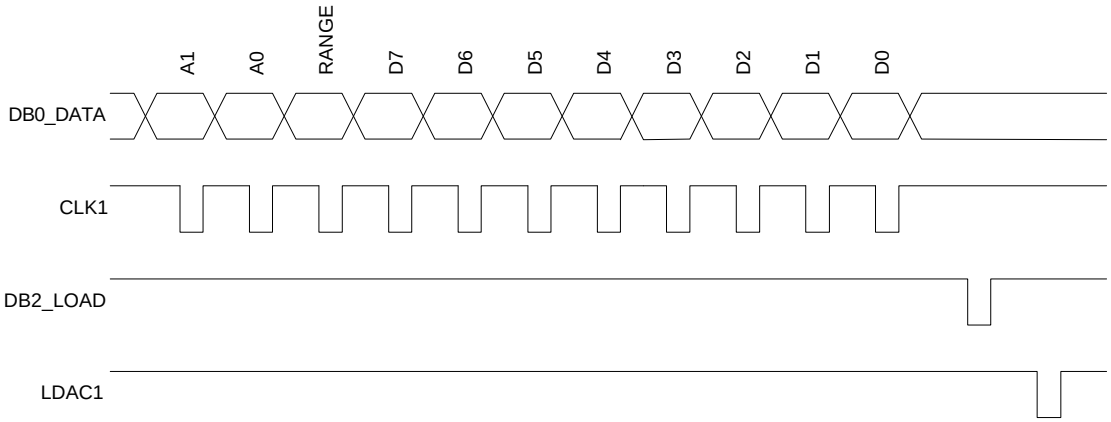
Raw data	Average missing samples	Average + Digital filter (FIR)
After 15 samples 		
After 20 samples 		
After 30 samples 		
After 40 samples 		
After 50 samples 		

D/A converter IC26

IC 26 is a quadruple 8-bit digital-to-analog converter (DAC). The output voltages of these DACs are set by serial data to pin 6 (DATA). The data is clocked into the DACs on each falling edge of pin 7 (CLK).
First two serial bits define the address of the DAC. Next bit defines the output voltage range; if '1' the range is from 0V to 5V, if '0' the range is 0V to 2.5V. The last 8 bits define the output voltage. The data is entered most significant bit (MSB) first.

Once all data bits have been clocked in, pin 8 (LOAD) is pulsed low to transfer the data from the serial input register to the selected DAC. Pin 13 (LDAC) is kept high during serial programming. The new value can be transferred to the DAC output by pulsing pin 13 (LDAC) low.

DAC function	Address bit		Range bit	Output pin
	A1	**A0**		
Trigger level	**0**	**0**	Ext. trig: **1** CH1, CH2 trig: **0**	12
Measure voltage of C46	**0**	**1**	**1**	11
CH1 Y-position	**1**	**0**	**1**	10
CH2 Y-position	**1**	**1**	**1**	9



Updating the D/A converter